ERRATA SHEET

Date: **August 20, 2002**
Document Release: **Version 1.1**
Devices Affected: **PXAG49**

This errata sheet describes both the functional deviations and any deviations from the electrical specifications known at the release date of this document.

Each deviation is assigned a number and its history is tracked in a table at the end of the document.

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Philips Semiconductors

PHILIPS

IDENTIFICATION:

The typical PXAG49 devices have the following top-side marking:

PXAG49xxx

xxxxxx

xxxYYWW R

The last letter in the third line (field 'R') will identify the device revision. This Errata Sheet covers the following revisions of the PXAG49:

Revision Identifier (R)	Comment
G, H	

Field 'YY' states the year the device was manufactured. Field 'WW' states the week the device was manufactured during that year.

FUNCTIONAL DEVIATIONS OF XA-G49

CORE.1: **End of Segment Return Error**

Introduction: Memory segments are divided into 64K blocks. The processor normally pre-fetches up to 16 bytes of code.

Problem: With an XA-G49 running in 16 bit mode out of external code space, the code fails if a RET instruction is located within 16 bytes of the end of a 64K segment. (xxfff0H - xxffffH) This absolute location may be affected by whatever code precedes the RET instruction, but the problem can occur anywhere in the last 16 bytes of a 64 kB segment.

No such failures have been observed when executing external code in 8-bit mode.

Workaround: Ensure that RET statements are not located within the last 16 bytes of a 64K segment. (e.g. by declaring these memory locations as reserved.)

ISP/IAP.1 **Automatic Block Erase during In-Application-Programming (IAP) doesn't erase all blocks.**

Problem: The Automatic Block erase during In-Application-Programming(IAP) doesn't erase all blocks, if the application is operating at a frequency > 12MHz, and the Watch Dog Timer (WDT) is enabled. (This problem does not occur at a frequency less than 12MHz or if the WDT is not used.)

Workaround: To erase block 2, 3, or 4, users can call the procedure "xaAutoBlockErase234" in the patch.

xaAutoBlockErase234: automatically erase and verify the block 2, 3, or 4 with error retry.

Input:	r6[15:13]: block address
Modified:	r0, r1, r2, r3, r4, r5, r6
On success:	CF=0 and R4L = 00H
On error:	CF=1 and R4L != 00H

ISP/IAP.2: **Erase / Erase Verify problem regarding Boot Vector (BPC) and Status Byte**

Introduction: The PXAG49 contains two special Flash registers: the BOOT VECTOR (BPC) and the STATUS BYTE. At the rising edge of reset, the PXAG49 examines the contents of the Status Byte. If the Status Byte is set to zero, power-up execution starts at location 0000H, which is the normal start address of the user's application code. When the Status Byte is set to a value other than zero, the contents of the Boot Vector is used as the high byte of the execution address and the low byte is set to 00H. The factory default setting is 0F8H, corresponding to the address 0F800H for the factory masked-ROM ISP boot loader. A custom boot loader can be written with the Boot Vector set to the custom boot loader. When erasing the Status Byte or Boot Vector, both bytes are erased at the same time. It is necessary to reprogram the Boot Vector after erasing and updating the Status Byte.

Problem: During the Erase operation, the Status Byte and the Boot Vector might not be erased thoroughly enough. Therefore, after the Status Byte and Boot Vector have been programmed, a read operation may deliver the wrong contents of these registers.

Workaround: Depending on the type of Flash programming, the following can be used:

Flash programming using an external Programmer:
Philips has notified the supported parallel programmer vendors.
Check with your programmer vendor to verify that their latest algorithm includes additional erase cycles for the Boot Vector and Status Byte.

Flash programming using ISP (In-System Programming):
The following ISP Flash programming tools are available with additional erase cycles for the Boot Vector and the Status Byte:
1) WinISP Version 2.29 (or higher, from Philips):
2) FlashMagic Version 1.31 (or higher, from Embedded Systems Academy)
(See next page how to download these tools.)

Flash programming using IAP (Application Program Interface):

The IAP call "erase boot vector", which also erases the status byte, must be called six times to ensure sufficient erasure of these bytes. (See AN716)

Free ISP software is available on the Philips web site: ”WinISP”, Version 2.29 (or later)

- Direct your browser to the following page:

  http://www.semiconductors.philips.com/products/standard/microcontrollers/download/80c51/flash/

- Download ”WinISP.exe”
- Execute WinISP.exe to install the software

Free ISP software is also available from the Embedded Systems Academy: ”FlashMagic”, Version 1.31 (or later)

- Direct your browser to the following page:

  http://www.esacademy.com/software/flashmagic/

- Download FlashMagic
- Execute ”flashmagic.exe” to install the software

How to download the ISP/IAP application note (AN716):

There is an application note available that deals with In-System and In-Application Programming of the XAG49.

At http://www.philipsmcu.com, search for AN716.

ERRATA HISTORY - FUNCTIONAL PROBLEMS

Functional Problem	Short Description	errata occurs in device revision
CORE.1	End of Segment Error	G, H
ISP/API.1	Automatic Block Erase during In-Application-Programming(IAP) doesn't erase all blocks.	G
ISP/IAP.2	Erase / Erase Verify problem regarding Boot Vector (BPC) and Status Byte	G